REMARKS

The Applicants thank the Examiner for the timely and favorable consideration of the submission filed on June 28, 2007.

In the Office Action, claims 12 to 22 were rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent No. 5,982,456 (hereinafter "Smith"). It is respectfully submitted, however, that Smith does not disclose all of the limitations of the rejected claims, as discussed in detail below.

Considering first the independent claim 12, the Office Action points to a description of the Digital Video Effects (DVE) unit 30 of Smith as allegedly disclosing the claimed integrated digital video effects processor having processing elements, to a description of the control processor 18 of Smith as allegedly disclosing the claimed one or more keyers, to elements 24 and 38 of Smith as allegedly disclosing the claimed one or more mixers, again to elements 24 and 38 and also to element 36 of Smith as allegedly disclosing the claimed one or more effects devices, and to the network card 28, the PCI bus 32, the Movie2 bus 34 and the switching unit 12 of Smith as allegedly disclosing the claimed routing elements. According to page 3 of the Office Action, the DVE unit 30, the PCI bus 32, the Movie2 bus 34, and the network card 28 allegedly disclose the claimed dedicated connection from the keyers, the mixers, the effects devices, and the routing elements to the processing elements of the digital video effects processor.

The Applicants respectfully submit that Smith does not disclose or suggest at least the claimed dedicated connection. Although Smith may disclose in very general terms that all of the elements shown in Figure 1 exist in one physical box, the cited reference does not disclose any direct connection between the DVE unit 30 and the internal mixing and keying elements. For example, the PCI bus 32 and the Movie2 bus 34 of Smith cannot reasonably be

characterized as dedicated connections. The Movie2 bus 34 is open-ended in Figure 1, and therefore clearly is intended to connect to other components. This bus is therefore not a dedicated connection. The PCI bus 32 is similarly open-ended at its right-hand end, and is connected to the memory 21 and to the general purpose processor 22 at its left-hand end. The elements 21 and 22 are clearly not digital video effects processors, keyers, mixers, effects devices, or routing elements, and therefore the PCI bus 32 of Smith also cannot be characterized as a dedicated connection.

Smith therefore fails to disclose at least the limitation "wherein the digital video effects processor has a dedicated connection from the keyers, the mixers, the effects devices, and the routing elements to the processing elements of the digital video effects processor", as explicitly recited in independent claim 12. The present application specifically shows links from within the multi-level effects (MLE) key routing (see Figure 2, items 94 and 95), with signals returning into the key routing paths (see Figure 2, items 91, 92, 96, 97), and switches (see Figure 2, items 61 to 63). The linkage of keying elements and a digital video effects processor unit (DVP), which is shown as element 5a in Figure 2, are described in the present specification at least at page 9, line 3 to page 10, line 2. This passage discusses switching the DVP 5a into and out of the key paths. The next paragraph of the specification, at page 10, lines 3 to 11, discusses alternate paths for different key types. At page 10, line 12 through page 11, line 2, advantages of this type of architecture, including allowing a keyer to seamlessly switch the DVP in and out, for example.

Independent claim 12 distinguishes over the cited reference for at least these reasons. Claims 13 to 22 depend from claim 12, and similarly distinguish over the cited reference. At least some of the dependent claims also define further distinguishing features.

Although claim 14 stands rejected as being disclosed at Column 3, lines 6 to 27 of Smith, it is noted that this claim recites that effects and memories of a DVE unit are recalled by a microprocessor and software. Smith does not appear to discuss memory recalls in any detail. The cited passage of Smith simply discloses that a storage unit can be coupled to processors for storing video signals.

Regarding claims 15 to 18, the Office Action refers to Column 4, lines 6 to 67 and to Column 3, lines 6 to 27. However, it would appear as though at least some of the features of these claims are not disclosed in Smith.

Claim 15, for example, has been amended for clarity, and now recites that video is routed from within a processing path of a multi-level effects device to the digital video effects processor, allowing partially composited signals to be processed by the digital video effects processor. There appears to be no mention in Smith of the processing of partially composited signals by an effects processor.

There also appears to be no mention in Smith of video within keyers being directly routed to a digital video effects processor, and the resultant video being routed back to the keyers. These features appear in claim 16. Smith appears only to disclose vague generalities of the DVE unit 30 being coupled to processors via buses. The cited reference appears to disclose only control processors, and not any specific video processing elements within the DVE unit 30.

Regarding claim 17, which has been amended for clarity, this claim recites dedicated keying resources to composite effects and transitions performed by the digital video effects processor, such that the one or more keyers of the switcher remain available for effects as determined by a user. The dedicated keying resources support this function without occupying the one or more keyers that the user can control to build effects. In Smith, there

appears to be no mention of such dedicated keying resources. Conventional systems such as the Smith system would require the use of a keyer for this function.

Smith also appears to be silent regarding a user interface to manipulate the digital video effects processor, wherein control of the digital video effects processor is fully integrated into the user interface, as recited in amended claim 18. Although Smith refers to the general purpose processor 22 as providing control signals, in response to operator inputs, that cause the other processing units (24, 26, 28, 30) to process selected input signals and generate a desired video output signal (see Column 4, lines 27 to 30), claim 18 specifically recites that control of the digital video effects processor is fully integrated into the user interface. Conventional implementations include DVEs and switchers as separate entities, and the present invention as defined in claim 18 improves on this through complete video and control integration.

Claims 20 and 21 stand rejected as being disclosed at Column 3, line 58 to Column 4, line 63 of Smith. Smith appears to simply state that all operations are synchronous to the video, providing real-time control. Smith does not appear to disclose any correlation between the control of switcher elements and the DVE unit 30. Claim 20 of the present application, on the other hand, recites means for allowing storage and recall of effects and memories on the video production switcher simultaneously with effects and memories of the digital video effects processor in an integrated manner. There also appears to be no discussion in Smith of pre-layering of effects, or the use of dedicated keying resources to composite a resultant digital effect, as recited in claim 21.

It is thus respectfully submitted that all of the claims 12 to 22 now pending in this application patentably distinguish over Smith for at least these reasons. Reconsideration and withdrawal of the anticipation rejections under 35 U.S.C. 102(e) are respectfully requested.

Respectfully submitted,

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